CLAIMS

The invention claimed is:

1. A circuit for interfacing between an image sensor and a processor, comprising:

a sampler operable to generate a plurality of analog image samples of an image by sampling a signal produced by the image sensor during a scanning of the image;

a Programmable Gain Amplifier operable to generate a plurality of amplified samples by employing an analog gain to amplify the analog image sample;

an Analog to Digital Converter operable to generate a plurality of digitized samples by digitizing the amplified samples; and

a Digital Programmable Gain Amplifier operable to generate amplified digitized samples for the processor by employing a digital gain to amplify the digitized samples, wherein the digital gain of the Digital Programmable Gain Amplifier at least overlaps the analog gain of the Programmable Gain Amplifier.

2. The circuit of Claim 1, further comprising a control signal that controls the analog gain and another control signal that controls the digital gain, wherein the digital gain at least overlaps the analog gain for each step along a range of the analog gain.

3. The circuit of Claim 2, wherein

the control signal employs a word with a number of bits that are substantially less than a number of bits in another word employed by the other control signal.

4. The circuit of Claim 1, wherein

a value of one of a control signal and another control signal is varied for the calibrating one of the Programmable Gain Amplifier or the Digital Programmable Gain Amplifier during which another value of the other one of the control signal and the other control signal is maintained relatively constant.

5. The circuit of Claim 1, wherein

generating the plurality of amplified digitized samples is performed within a dynamic range that is at least as large as a dynamic range of any one resolution step defined by generating the plurality of amplified image samples.

6. The circuit of Claim 1, wherein the image sensor includes at least one of a charge coupled device (CCD) array and a diode.

7. The circuit of Claim 1, wherein the processor is a digital image processor that is operable for a scanning system.

8. The circuit of Claim 1, wherein one of a plurality of calibration algorithms are employed to calibrate the operation of the Programmable Gain Amplifier and the Digital Programmable Gain Amplifier prior to the generation of the plurality of amplified digitized samples for each scanned image.

9. The circuit of Claim 1, further comprising a calibrator operable to calibrate each of the Programmable Gain Amplifier and the Digital Programmable Gain Amplifier prior to the generation of the plurality of amplified digitized samples for the processor.

10. A method for interfacing between an image sensor and a processor, comprising:

generating a plurality of analog image samples by sampling a signal produced by the image sensor during the scanning of an image;

generating a plurality of amplified samples by amplifying the plurality of analog image samples with an analog gain;

generating a plurality of digitized samples by digitizing the plurality amplified samples; and

generating a plurality of amplified digitized samples for the image processor by amplifying the digitized samples with a digital gain, wherein the amplified digitized samples are provided to the processor for processing of the scanned image.

11. The method of Claim 10, further comprising controlling the analog gain and controlling the digital gain, wherein the digital gain at least overlaps the analog gain over a range of the analog gain.

12. The method of Claim 10, further comprising varying a value for calibrating one of the analog gain and the digital gain during which another value for calibrating the other one of the analog gain and the digital gain is maintained relatively constant.

13. The method of Claim 10, wherein

generating the plurality of amplified digitized samples is performed within a dynamic range that is at least as large as a dynamic range of any one resolution step defined by the generation of the plurality of amplified image samples.

14. The method of Claim 10, wherein one of a plurality of calibration algorithms are employed to calibrate the operation of the analog gain and the digital gain prior to the generation of the plurality of amplified digitized samples for each scanned image.

15. The method of Claim 10, further comprising calibrating each of the analog gain and the digital gain prior to the generation of the plurality of amplified digitized samples for the processor.

16. The method of claim 15, further comprising

adjusting the digital gain until it is calibrated while the analog gain is held at a predetermined value; and

adjusting the analog gain until it is calibrated while the digital gain is held at its calibrated value.

17. The method of claim 15, further comprising

adjusting the analog gain until it is calibrated while the digital gain is held at a predetermined value; and

adjusting the digital gain until it is calibrated while the analog gain is held at its calibrated value.

18. A circuit for interfacing between an image sensor and a digital image processor, comprising:

a means for generating a plurality of analog image samples by sampling a signal produced by the image sensor during the scanning of an image;

a means for a Programmable Gain Amplifier to generate a plurality of amplified samples by amplifying the analog image sample;

a means for an Analog to Digital Converter to generate a plurality of digitized samples by digitizing the amplified samples;

a means for a Digital Programmable Gain Amplifier to generate amplified post-digitized samples for the image processor by digitally amplifying the digitized samples; and

a means for calibrating each of the Programmable Gain Amplifier and the Digital Programmable Gain Amplifier prior to the scanning of each image.